REMARKS

Prior to entry of the instant amendment, claims 1-14 are pending in the subject application. By the instant amendment, claims 1-3, 6, 11, and 12 are amended; and claims 4, 5, 7, 8, and 10 are canceled without prejudice to or disclaimer of the subject matter contained therein. No new matter is added. Claim 1 is the sole independent claim

Claims 1-3, 6, 9, and 11-14 are presented to the Examiner for further prosecution on the merits. Favorable reconsideration of this application, in light of the preceding amendments and following remarks, is respectfully requested.

Objections to the Claims

Claims 3 and 12 stand objected to due to informalities. By the instant amendment, Applicants have amended claims 3 and 12, taking into consideration the Examiner's comments, to obviate the objections. Withdrawal of the objections is respectfully requested.

Claims Rejections - 35 U.S.C. § 103

Claims 1 and 9-10 stand rejected under 35 U.S.C. § 103(a) as being unpatentable over U.S. Patent No. 6,851,618 ("Halope"). Applicant respectfully traverses this rejection for the reasons discussed below.

In order to establish a *prima facie* case of obviousness under 35 U.S.C. § 103(a), all of the claim limitations of the rejected claims must be described or suggested by the cited document(s).[1] Applicants respectfully submit that the cited documents do not meet this criteria, because no modification of the Halope reference will describe or

suggest all of the claim limitations of rejected claims 1 and 9-10, and therefore, a *prima facie* case of obviousness has not been established.

For example, claim 1, as amended, recites, *inter alia*:

> a process for assembling at least one electronic component made up of a chip provided with contacts on one of the faces of the chip, said contacts being set off on a conductive film constituting flat conductive areas that extend the contacts of the chip in a plane over the chip, the conductive areas being connected to conductive tracks placed on a surface of a planar insulating substrate.

The Halope reference merely discloses an electronic module made up of a chip mounted on a double sided circuit. The shape of the cavity is adapted to receive the chip in a smaller central part while the double sided circuit fits in an upper larger part of the cavity (*see col. 3 lines 18-25*). By contrast, the claimed invention discloses that the cavity receives only the chip and the conductive areas connected to the contacts of the chip that are applied against the substrate in a zone surrounding the cavity. Such a configuration allows a connection of the conductive areas on tracks located on a second substrate superimposed on the substrate provided with the cavity.

In addition, the Halope reference discloses that the double sided circuit of the module flushes the surface of the substrate and is intended to form external contacts of a card. However, it is submitted that no second substrate provided with conductive tracks entering in contact with the double sided circuit is disclosed.

Moreover, FIGS. 4 to 6 of Halope disclose that the module is glued in the cavity and rigidly maintained into PVC material which is previously melted during a hot laminating process of the layers forming the card body. Accordingly, openings in the vicinity of the electronic module reinforce the connection of the module and the link between the internal layers (*see col. 4, lines 50 - 54*). In contrast, the claimed

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[1] See *In Re Royka*, 490 F.2d 981, 180 USPQ 580 (CCPA 1974). See also MPEP § 2143.03.

invention discloses that the insulating layer is laminated on the substrate allowing the contacts to rub together when repeated stresses are exerted on the substrate. That is, using filling material passing through holes, as taught by the Halope reference, reinforces the rigidity of the module connection so that the pressed contacts surfaces cannot rub together. Therefore, the Halope reference fails to disclose or suggest, "the conductive areas of the electronic component and the conductive tracks of the substrate are in contact to achieve an electric connection via a pressure of application of the insulating material layer on the electronic component, and configured to rub together when repeated stresses are exerted on the substrate," as recited in claim 1.

In view of the above, Applicant respectfully submits that the Halope reference fails to teach or suggest each and every element of claim 1, and therefore, claim 1 is allowable over the cited prior art. Claims 9 and 10 are dependent from claim 1, and therefore, also allowable. Accordingly, Applicant respectfully requests that the rejection under 35 U.S.C. § 103(a) be reconsidered and withdrawn.

Claims 2-8 and 11-14 are rejected under 35 U.S.C. § 103(a) as being unpatentable over Halope in view of U.S. Patent No. 5,598,032 ("Fidalgo"). Applicant respectfully traverses this rejection for the reasons discussed below.

Applicant respectfully submits that claims 2-8 and 11-14 are believed to be allowable for at least the reasons set forth above regarding claim 1. Since claims 2-8 and 11-14 are patentable at least by virtue of their dependency on claim 1, Applicants respectfully request that the rejection of claims 2-8 and 11-14 under 35 U.S.C. § 103(a) be withdrawn.

In addition, the Fidalgo reference fails to provide the teachings noted above as missing from the Halope reference. In particular, the Fidalgo reference discloses that the extensions of the contacts of the chip forming the electronic module are made up of wires or conductive tapes folded on the lateral faces of the electronic module so that the chip contacts of one face of the module are brought to the opposite face. Therefore, a configuration where the electronic module or component having a chip provided with "contacts set off on a conductive film constituting flat contact areas that extend the contacts of the chip in a plane over the chip," as recited in claim 1, is not disclosed in the Fidalgo reference.

Further, in the Fidalgo reference, the connections of the electronic module are made rigidly with conductive bonder (see col. 6, lines 12-16), i.e., the rigid connections do not allow a friction of both surfaces in contact when the card is deformed at the place of the electronic module. Therefore, a constraint on this type of connection leads to breaking either of the track segment on the substrate or via the gluing of the segment on the module contact. The Fidalgo reference, thus, fails to disclose, or even suggest, the feature of contacting the conductive areas of the electronic component and the conductive tracks of the substrate made by pressure and rubbing between the contact surfaces on the substrate and on the electronic component.

For at least these reasons, Applicant respectfully submits that claims 2-8 and 11-14 are allowable. Accordingly, reconsideration and withdrawal of the rejection under 35 U.S.C. § 103(a) are respectfully requested.

CONCLUSION

In view of the above remarks and amendments, Applicant respectfully submits that each of the pending objections and rejections has been addressed and overcome, placing the present application in condition for allowance. A notice to that effect is respectfully requested. Further, the above remarks demonstrate the failings of the outstanding rejections, and are sufficient to overcome the rejections. However, these remarks are not intended to, nor need they, comprehensively address each and every reason for the patentability of the claimed subject matter over the applied prior art. Accordingly, Applicant does not contend that the claims are patentable solely on the basis of the particular claim elements discussed above.

Should there be any outstanding matters that need to be resolved in the present application, the Examiner is respectfully requested to contact the undersigned at the telephone number below.

If necessary, the Commissioner is hereby authorized in this, concurrent, and future replies, to charge payment or credit any overpayment to Deposit Account No. 08-0750 for any additional fees required under 37 C.F.R. § 1.16 or under 37 C.F.R. § 1.17; particularly, extension of time fees.

Respectfully submitted,

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By _____

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